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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

WESTERN DIVISION

CREATIVE INTEGRATED SYSTEMS, INC.,

Plaintiff,

v.

NINTENDO OF AMERICA INC.; NINTENDO CO., LTD.; and MACRONIX INTERNATIONAL CO., LTD.,

Defendants.

Case No. 2:10-CV-2735 PA (VBK)

DEFENDANTS' MOTION FOR JUDGMENT AS A MATTER OF LAW OF NO INFRINGEMENT

Trial: March 4, 2014
Courtroom: 15

Judge: Hon. Percy Anderson

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Defendants Nintendo of America Inc., Nintendo Co., Ltd., and Macronix International Co., Ltd. ("Defendants") respectfully submit this memorandum in support of its motion for judgment as a matter of law ("JMOL") of noninfringement under Fed. R. Civ. P. 50(a).

I. LEGAL STANDARD

A. Judgment as Matter of Law

Under Rule 50(a), "[i]f a party has been fully heard on an issue during a jury trial and the court finds that a reasonable jury would not have a legally sufficient evidentiary basis to find for the party on that issue, the court may: (A) resolve the issue against the party; and (B) grant a motion for judgment as a matter of law against the party on a claim or defense that, under controlling law, can be maintained or defeated only with a favorable finding on that issue." Fed. R. Civ. P. 50(a)(1).

B. Direct Infringement

Direct, literal infringement is established only if Plaintiff establishes that "every limitation recited in the claim appears in the accused device, i.e., when the properly construed claim reads on the accused device exactly." *DeMarini Sports, Inc. v. Worth, Inc.*, 239 F.3d 1314, 1331 (Fed. Cir. 2001) (quotations omitted).

C. Inducement

To establish active inducement under Section 271(b), the plaintiff must prove that the accused infringer acted with a culpable state of mind, including proving that the accused infringer (1) acted with knowledge of the patent and knowledge that the induced acts constitute infringement; or (2) was willfully blind to the existence of at least one of the Patents-in-Suit, at that time, and infringing nature of the induced acts. *Commil USA, LLC v. Cisco Sys.*, 720 F.3d 1361, 1367 (Fed. Cir. 2013) (*citing Global-Tech Appliances, Inc. v. SEB S.A.*, 131 S. Ct. 2060, 2068 (2011)). Further, "evidence of an accused inducer's good-faith belief of invalidity may negate the requisite intent for induced infringement." *Id.* at 1368-69.

II. NO DIRECT INFRINGEMENT.

A. The Derivative Memory Array does not have a first means and a second means that are coupled to the same diffusion bit line at opposite ends of a block, as required by claims 5-7.

Claims 5, 6, and 7 require that the first and the second means are connected to the ***same*** diffusion bit line. In particular, claim 5, in relevant part, reads as follows:

> *first means* for selectively coupling said at least one virtual ground line *to* ***one of said diffusion bit lines*** within each block, said first means coupled to one end of said addressed block of memory cells;
>
> *second means* for selectively coupling ***said one diffusion bit line*** to said main bit line within each block, said second means coupled to the opposite end of said addressed block from said first means . . .

'497 Patent at 39:10-18 (emphasis added). During his cross-examination, Plaintiff's expert, Mr. Dennis Wilson, testified that the first and second means allegedly found in the Derivative Memory Array are connected to different diffusion bit lines. In particular, Mr. Wilson testified as follows:

> Q. Mr. Wilson there's -- I'm showing you another slide from your presentation. This is the derivative memory array. Do you recognize it?
>
> A. Yes, sir.
>
> Q. Here you labelled a number of lines -- well, the entire box -- you've got a text box that says, "Said columns of memory cells being coupled together by diffusion bit lines." Do you see that?
>
> A. Yes, sir.
>
> Q. And you do agree those are diffusion bit lines that you've labelled there; right?

A. Yes, sir.

Q. And there are -- I'm showing you another slide from your demonstrative. It shows -- it shows a couple of those diffusion bit lines; right?

A. Yes, sir.

Q. And at the top this -- this slide also shows a -- an arrow pointing to a transistor; correct?

A. Yes, sir.

Q. And that transistor is labelled the -- here as the first means; is that --

A. Yes.

Q. And and on another slide of your same demonstrative, there's the same path -- you've highlighted a red path through this block of cells; right?

A. Yes, sir.

Q. You would call that a transmission path?

A. Yes, sir.

Q. And at the other end of that -- and coupled in line with that same path there's another transistor, and I think that you're implying that's a second means; correct?

A. That is a second means.

Q. And that second means is -- on the left side of that second means transistor there's a diffusion bit line; right?

A. Correct.

Q. And do you -- and on the left side of the transistor you've identified as the first means transistor at the top, ***there's another diffusion bit line; right?***

A. That's correct.

Q. Those aren't the same diffusion bit lines; right?

A. No, sir.

Q. So the first means at one end of the array is -- would you say it's coupled to a diffusion bit line?

A. Yes, sir.

Q. And the second means at the bottom end of the array is coupled to a different diffusion bit line?

A. Yes, sir.

Trial Tr. of March 6, 2014, Vol. I at 99:13-101:9 (emphasis added). Accordingly, because Mr. Wilson admitted that the first means and the second means are coupled to different diffusion bit lines in the accused Derivative Memory Array, Plaintiff has not met its burden of presenting a sufficient evidentiary basis to show that the Derivative Memory Array infringes claim 5. Claims 6 and 7 depend from 5, and incorporate each of the limitations recited in claim 5. As such, Plaintiff has not met its burden of presenting a sufficient evidentiary basis to show that the Derivative Memory Array infringes claims 6 and 7.

B. Plaintiff has failed to establish that the Standard Memory Array includes a "first means" for selectively coupling said at least one *diffusion* virtual ground line to one of said diffusion bit lines within each block, as required by claims 5, 6, and 7.

Claim 5 of the '497 Patent, in relevant part, requires a first means that selectively couples a ***diffusion virtual ground line*** to a diffusion bit line. In particular, claim 5 reads as follows:

> **5.** An improvement in a memory circuit having a plurality of addressable memory cells arranged in a plurality of blocks, each block of said plurality of memory cells being logically organized in columns, said columns of memory cells being coupled together by diffusion bit lines, said

> memory block being provided with ***at least one diffusion virtual ground line*** and a diffusion main bit line which with said diffusion bit lines define a length of said block, said block having opposing ends at opposite ends of said length, said plurality of blocks being coupled together at their ends by metallization lines, said improvement comprising:
>
> first means for selectively coupling ***said at least one virtual ground line to one of said diffusion bit lines within each block***, said first means coupled to one end of said addressed block of memory cells . . .

'497 Patent at 38:66-39:24 (claim 5). During his direct examination, Plaintiff's expert testified that the "first means" in the Standard Memory Array selectively couples "at least one virtual ground line, ***which is the metal line*** to one of said diffusion bit lines within each block." Trial Tr. of March 5, 2014, Vol. I, at 101:1-3. This testimony puts the Standard Memory Array outside the scope of claims 5-7, because those claims require that the first means selectively couples a ***diffusion*** virtual ground line to a diffusion bit line. Similarly, with respect to the Derivative Memory Array, Mr. Wilson testified that the first means "couples the lines together to the diffusion virtual ground line, which is ***metal wire contact there***." In particular, Mr. Wilson testified as follows:

> Q. Did you find whether the first means for selectively coupling said at least one virtual ground line to one of said diffusion bit lines within each block. "Said first," means coupled to one end of said address block of memory cells?
>
> A. Yes, I did.
>
> Q. Did you find that element in the accused Macronix ROM chips?
>
> A. Yes, I did.

> Q. Could you show the jury where you found that?
>
> A. Okay. So there's the more detailed -- same thing he just read about the first means. And we talked about this means plus function. So here that transistor there and the control line, we identified -- we had a CB and a CA -- and we said transistors were connected to them. That transistor there, it's coupling -- whenever there's a transistor highlighted by the yellow rectangle, it's connecting those two diffusion lines together. So it's connecting the diffusion line on the right of it to the one on the left which goes down and has the little T-shape on the bottom to the contact, ***so I have a first means. Selectively coupling at least one virtual ground line, which is the metal line to one of said diffusion bit lines within each block***. Said first means coupled to one end of said address block --

Id. at 100:7-101:4. Accordingly, because Plaintiff has failed to establish that the Standard Memory Array includes a "first means" that selectively couples a ***diffusion*** virtual ground line to a diffusion bit line, Plaintiff has failed to meet its burden of presenting a sufficient evidentiary basis to show that the Standard Memory Array infringes claims 5, 6, and 7 of the '497 Patent.

C. Mr. Wilson assumed, but did not prove, that the accused Derivative Memory Array includes the "virtual ground lines" recited in claims 5-7 and 12.

Mr. Wilson testified that he assumed that the accused Derivative Memory Array includes the "virtual ground lines" that are required by the asserted claims. Trial Tr. of March 6, 2014, Vol. I, at 47:14-23. In particular, Mr. Wilson testified as follows:

> Q. Do you see any virtual ground lines in Exhibit 335?
>
> A. Yes.
>
> Q. Could you identify them for me.
>
> A. At the top of the drawing there are two U shaped structures,

a G-0 and a G-1.

Q. All right. Stops there; right?

A. Correct.

Q. And there's another one right here?

A. Correct.

Q. That one stops right there; right?

A. Correct.

Q. And then below those virtual ground lines there are -- that's where the columns of memory cells are in this circuit?

A. Correct.

Q. I'm going to draw a box around those. There are one, two, three, four, five, six, seven, eight -- eight columns of memory cells there as well. Okay. So these -- these two upside down U's you've identified as virtual ground lines; right?

A. Yes, I have.

Q. So I'm going to label that VGL-1. This one VGL-2.

A. I don't think your picture is quite on the screen.

Q. Oh, you're right.

A. You might want to shrink it just a tad.

Q. And Mr. Wilson, how do you know those two lines you've identified are virtual ground lines?

A. I had to make an assumption that those are virtual ground lines based on the label G, similar to previous ones. It's also in the layout labelled as G, which I'm assuming refers to ground.

Q. Is it your opinion that these -- these lines are full-time connected to ground or sometimes connected to if, in other words, if those lines were full-time connected to ground would they just be called ground lines instead of virtual ground lines?

A. If they were full-time connected to the ground?

Q. Yes.

A. Probably just call them ground lines.

Trial Tr. of March 6, 2014, Vol. I, at 46:15-48:5. Mr. Wilson further testified as follows:

Q. Mr. Wilson, I didn't ask if -- how you can distinguish those virtual ground line from main bit lines. So maybe I need a little clarification.

I asked how you could tell that they were virtual ground lines or just ground lines.

A. Without seeing the external circuitry, I couldn't tell.

Q. And have you seen the external circuitry?

A. I have not.

Q. Have you asked to see the external circuitry?

A. I have not.

Id. at 49:3-12.

Accordingly, Plaintiff failed to present evidence that the Derivative Memory Array includes the claimed "virtual ground lines" of claims 5, 6, 7, and 12. As such, Plaintiff has failed to meet its burden of presenting a sufficient evidentiary basis to show that the Derivative Memory Array infringes claims 5-7 and 12 of the '497 Patent.

D. Plaintiff has failed to establish that the Standard Memory Array has a first means that couples a virtual ground line to a diffusion bit line, as required by all of the asserted claims.

All of the asserted claims have the requirement, albeit with slight differences in language, of a first means for selectively coupling a virtual ground line to a diffusion bit line. During his cross-examination, Plaintiff's expert admitted that the first means he alleges is found in the accused Standard Memory Array products couples one diffusion bit line to another diffusion bit line, rather than coupling a virtual ground

line to a diffusion bit line. *See* Trial Tr. of March 6, 2014, Vol. I, at 94:1-96:1. In particular, Mr. Wilson testified as follows:

> Q. First means transistor couples that diffusion bit line to the left to that diffusion bit line on the right; correct?
>
> A. Yes, sir.
>
> Q. In fact, it selectively couples; right? Because it's a transistor, sometimes it can turn on, sometimes it can turn off?
>
> A. Yes, sir.

Id. at 95:20-96:1. As such, Plaintiff has failed to meet its burden of presenting a sufficient evidentiary basis to show that the Standard Memory Array infringes claims 5-7 and 12 of the '497 Patent.

E. Plaintiff has failed to establish that both the Standard Memory Array and the Derivative Memory Array have "columns of memory cells being coupled together by . . . at least one virtual ground line" as required by claim 12.

Claim 12 requires that columns of memory cells are "coupled together by diffusion bit lines, at least one virtual ground line, ***and*** a main bit line." '497 Patent at 40:68-41:2 (emphasis added).

Mr. Wilson did not present any evidence that the Derivative Memory Array and the Standard Memory Array has columns of memory cells being coupled together by all three: (1) diffusion bit lines, (2) at least one virtual ground line, and (3) a main bit line, as required by claim 12. Trial Tr. of March 5, 2014, Vol. II, at 120:5-124:1.

At best, Mr. Wilson assumed that both the Standard Memory Array and the Derivative Memory Array include "at least one virtual ground line." *Id.* at 122:14-123:16. Just because Mr. Wilson attempted to establish that the Standard Memory Array and the Derivative Memory Array include "at least one virtual ground line", that does not mean that the columns of memory cells in both the Standard and Derivative

Memory Array are "***coupled together by*** . . . at least one virtual ground line." Mr. Wilson ignores this requirement of claim 12.

Because Mr. Wilson failed to present any evidence that the columns of memory cells are "***coupled together*** . . . by at least one virtual ground line," Plaintiff has failed to meet its burden of presenting a sufficient evidentiary basis to show that both the Standard Memory Array and the Derivative Memory Array infringe claim 12.

Further, Plaintiff's expert Mr. Wilson admitted that in the Derivative Array the lines he alleges are virtual ground lines do not even reach the columns of memory cells:

> Q: Mr. Wilson, I'm showing you claim 12 form your presentation. You agree that this claim -- I'm look at about the fifth line down in claim 12 -- that this claim requires columns of memory cells being coupled together by diffusion bit lines?
>
> A. Yes, sir.
>
> Q. You agree that it requires columns of memory cells being coupled together by at least one virtual ground line?
>
> A. Yes, sir.
>
> Q. Showing you exhibit 1066, Mr. Wilson, the line that you've identified as VGL1 doesn't touch the columns of memory cells that we've identified in this exhibit, correct?
>
> A. I can't answer that.
>
> Q. Well, sir, I'm asking if that line that we've highlighted -- we've highlighted a line, right?
>
> A. Yes, sir.
>
> Q. That line is in the shape of a -- kind of an upside down U, right?
>
> A. Yes, sir.
>
> Q. And it stops at two n's, right? On the bottom?

A. Your brown line does not connect down to the memory cells, that's correct.

Q. The line we've labeled VGL1 does not touch the memory cells, correct?

A. On your drawing, that's correct.

Q. The line we've labeled as VGL2 does not touch the columns of memory cells, correct?

A. That's also correct.

See Trial Tr. of March 6, 2014, Vol. II at 5:1 to 6:3. Accordingly, for at least the foregoing reasons, Plaintiff has failed to meet its burden of presenting a sufficient evidentiary basis to show that the Derivative Memory Array infringes claim 12.

F. Plaintiff has failed to establish that the Standard Memory Array includes the limitation "with completion of the circuit through said addressed memory cell through said first means to said virtual ground line" as required by claims 6 and 7.

Claim 6, with the relevant portion highlighted in bold, reads as follows:

6. The improvement of claim 5 wherein one of said blocks of memory cells is comprised of a plurality of columns of memory cells, said first means being coupled to two of said columns while said second means is coupled to another two of said plurality of columns, two diffusion lines corresponding to each column of said memory cells, said first means for selectively shorting together two corresponding diffusion lines corresponding to columns selected by said first and second means respectively, an addressable memory cell being read through said main bit line selectively coupled to said addressable memory cell through said second means ***with completion of the circuit through said addressed memory cell through said first***

> ***means to said virtual ground line***.

'497 Patent at 39:25-39 (emphasis added). With respect to this limitation of claim 6, Mr. Wilson testified as follows during his cross-examination:

> Q. This -- this transmission path, this circuit has gone through the second means up at top, right?
>
> A. For this transistor to be access to it, it would have had to go through the second means. That's correct.
>
> Q. And then it has come down from the other side of the second means through the block to here, right?
>
> A. That's correct.
>
> Q. So the transmission path has come from the second means through diffusion bit line till it reaches the memory cell, right?
>
> A. Correct.
>
> Q. Then the transmission path goes through the memory cell, right?
>
> A. Correct.
>
> Q. And at that point it has reached virtual ground line?
>
> A. That's correct.
>
> Q. Claim 6 language that you've said here says, "with completion of the circuit through said address memory cell through said first means to said virtual ground line," right?
>
> A. Correct.
>
> Q. But this is -- this transmission path you've just agreed has already reached the virtual ground line and the first means is clear down here, correct?
>
> A. Correct.

See Trial Tr. of March 6, 2014, Vol. II at 20:8-21:6 and at 16:8-21:16; Ex. 1067. As such, Plaintiff has failed to meet its burden of presenting a sufficient evidentiary basis

to show that the Standard Memory Array infringes claims 6 and 7.

III. NO INDUCEMENT.

A. Granting JMOL of No Direct Infringement Requires a Finding of No Inducement.

Indirect infringement, whether inducement to infringe or contributory infringement, can only arise in the presence of direct infringement. *See Dynacore Holdings Corp. v. U.S. Philips Corp.*, 363 F.3d 1263, 1272 (Fed. Cir. 2004). Accordingly, to the extent the Court grants JMOL of no direct infringement, it should also grant JMOL of no inducement.

B. Plaintiff introduced no evidence that Defendant Macronix International Co., Ltd. knew of the '497 Patent.

Defendants move for judgment as a matter of law because Plaintiff failed to introduce any evidence that Defendant Macronix International Co., Ltd. ("MXIC") knew of the '497 Patent. As noted above, Plaintiff bears the burden of showing inducement. Further, as noted above, inducement requires Plaintiff to prove that the accused infringer (1) acted with knowledge of the patent and knowledge that the induced acts constitute infringement; or (2) was willfully blind to the existence of at least one of the Patents-in-Suit, at that time, and infringing nature of the induced acts. Here, Plaintiff has established neither prong. Accordingly, the Court should grant Defendants' JMOL of no inducement as to MXIC.

C. Plaintiff introduced no evidence that Defendant Nintendo Co., Ltd. induced the infringement of Nintendo of America Inc.

As noted above, inducement requires Plaintiff to prove that the accused infringer (1) acted with knowledge of the patent and knowledge that the induced acts constitute infringement; or (2) was willfully blind to the existence of at least one of the Patents-in-Suit, at that time, and infringing nature of the induced acts. Here, Plaintiff has established neither. Accordingly, the Court should grant Defendants' JMOL of no inducement as to Nintendo Co., Ltd. ("NCL").

IV. CONCLUSION

For the foregoing reasons, Defendants move for judgment as a matter of law of (1) no direct infringement and (2) no inducement as to MXIC and NCL.

Dated: March 12, 2014

Respectfully submitted:

BAKER & McKENZIE LLP

By: /s/ Daniel A. Tallitsch
Daniel A. Tallitsch

Attorneys for Defendants Nintendo of America Inc., Nintendo Co., Ltd., and Macronix International Co., Ltd.